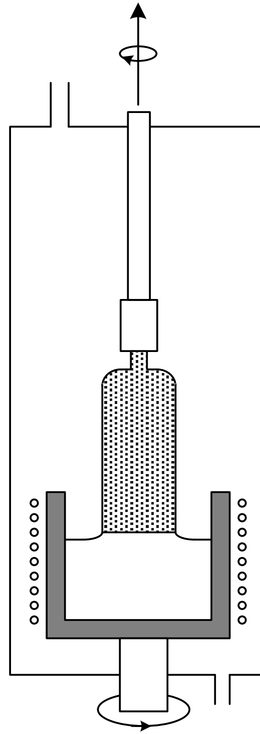
Semiconductor Technology

from A to Z



Wafer fabrication

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1 Wafer fabrication

1.1 Properties of silicon

Silicon is the chemical element with the atomic number 14 in the periodic table of the elements. Silicon is a classic semiconductor, its conductivity lies between that of conductors and dielectrics. Naturally silicon (from the latin silex/silicis: pebbles) occurs only as oxide: silicon dioxide (SiO_2) in form of sand, quartz, or silicate (compounds of silicon with oxygen, metals and others). Thus silicon is a very cheap starting material, whose value is determined with further processing. Other semiconductors such as germanium or gallium arsenide compound semiconductors offer substantially improved electrical properties than silicon: the charge carrier mobility and thus the resulting switching speeds are significantly higher in germanium and GaAs. However, silicon has significant advantages in contrast to other semiconductors.

On a silicon crystal oxide layers can be produced very easily, the resulting silicon dioxide is an insulator of highest quality which can be fabricated precisly on the substrate. To create similar insulators on germanium or gallium arsenide is very expensive. The possibility to change the conductivity by doping silicon is another big advantage. Other substances are in part very toxic, and compounds with these elements are not as durable and stable as in silicon. Requirement for the use of silicon in semiconductor manufacturing is that the silicon is present in an ultrapure form as single crystal. This means that the silicon atoms in the crystal lattice are regularly arranged and there are absolutely no undefined impurities in the material.

In addition to the single crystal, there is polysilicon (poly = many) and amorphous silicon (a-Si). While the single crystal silicon is the basis for microelectronics in form of circular wafers, the polycrystalline silicon is suitable to fulfill specific tasks (e.g. masking, gate electrode, ...). Polysilicon is made up of many individual irregularly arranged single crystals, and can be deposited and patterned very easily. Amorphous silicon does not have a regular but a disordered lattice structure and plays no role in semi-

conductor manufacturing, but amorphous silicon offers advantages over other forms of silicon in the manufacture of thin film solar cells.

1.2 Raw silicon

1.2.1 Production of raw silicon

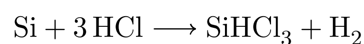
Silicon as it is used in semiconductor manufacturing, is made up of quartz. Oxygen which reacts very fast with silicon even at room temperature, and which is present in quartz associated with silicon as silicon dioxide SiO_2, must be removed. This is done just above the melting point of silicon (1414 °C) in furnaces using carbon. At 1460 °C oxygen cleaves of the silicon and reacts with carbon C to carbon monoxide CO:

$$SiO_2 + 2\,CSi \longrightarrow 2\,CO$$

Iron prevents the reaction of silicon and carbon to form silicon carbide. At these temperatures the carbon monoxide is in gaseous state and can be separated from the molten silicon easily. However, the raw silicon is still heavily polluted. There are up to 5 % impurities, such as for example iron, aluminum, phosphorus, and boron. These substances must be removed in additional processes.

1.2.2 Purification of the raw silicon

Using a trichlorosilane process many impurities are filtered out by distillation. The raw silicon and hydrogen chloride HCl react at about 300 °C to form gaseous hydrogen H_2 and trichlorosilane $SiHCl_3$:

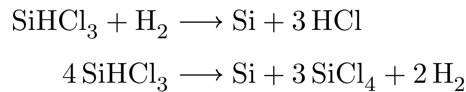


$$Si + 3\,HCl \longrightarrow SiHCl_3 + H_2$$

The contaminants which also react with the chlorine, need higher temperatures to transfer in the gaseous state. This allows separation of the trichlorosilane. Only car-

bon, phosphorus, and boron, which have similar condensation temperatures, can not be filtered out in this process.

The trichlorosilane process can be reversed, so that the purified silicon condeses in polycrystalline form. This is done at approximately 1100 °C by adding hydrogen inside a quartz chamber, in which thin silicon rods are placed:



$$SiHCl_3 + H_2 \longrightarrow Si + 3\,HCl$$
$$4\,SiHCl_3 \longrightarrow Si + 3\,SiCl_4 + 2\,H_2$$

The silicon reflects on the silicon rods which grow to bars with a diameter of more than 30 mm. This polysilicon could already be transformed into a single crystal using the Czochralski process, however, the degree of purity for semiconductor manufacturing is still not high enough.

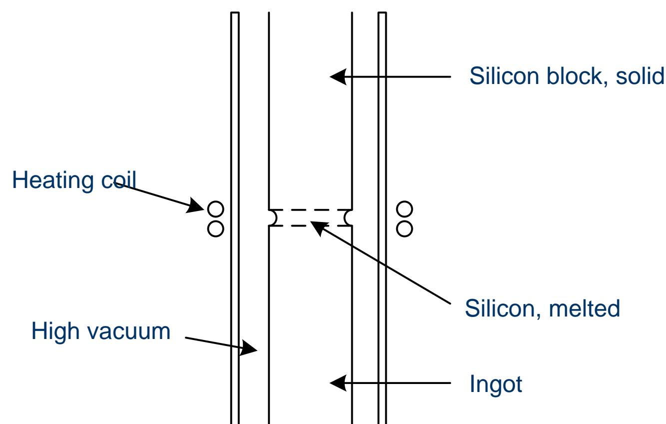


Fig. 1.1: Illustration of the zone cleaning process

1.2.3 Zone cleaning

To increase the purity once more a cleaning process is used. Thereby a high frequency coil is placed around the silicon rod to melt the silicon bars, and therefore the contaminations accumulate at the bottom due to higher solubility in the liquid phase; the surface tension of the silicon prevents the melt to flow out. By multiple repetition of this procedure, the content of impurities in silicon is further reduced and thus it can be

used for fabrication of the single crystal. To prevent further contamination, all of the processes are made under a vacuum atmosphere.

At the end of these processes the silicon has a purity of more than 99,9999999 %, which means that there is less than 1 foreign atom per 1 billion silicon atoms.

1.3 Fabrication of the single crystal

1.3.1 The single crystal

A single crystal (monocrystal), as it is required in semiconductor manufacturing, is a regular arrangement of atoms. There are polycrystalline (composition of many small single crystals) and amorphous silicon (disordered structure). Depending on the orientation of the lattice, silicon wafers have different surface structures which impact various properties as the charge carrier mobility or the behaviour in wet-chemical anisotropic etching of silicon.

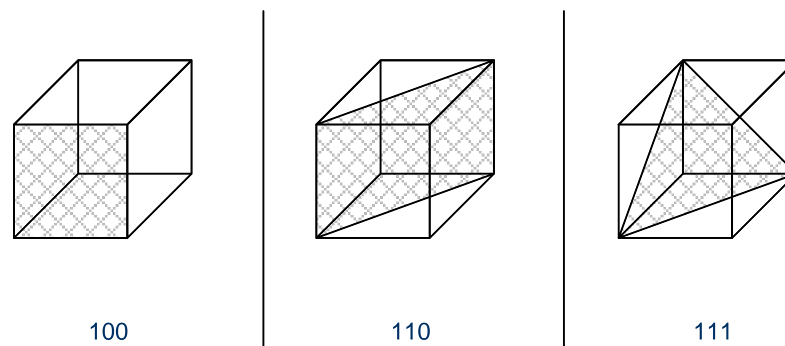


Fig. 1.2: Crystal orientation

In micromechanics the crystal orientation is of particular importance. It allows microchannels with perpendicular walls on (110) silicon, whereas flank angles of 54.74° are possible on (100) orientation.

1.3.2 Czochralski process

The polycrystalline silicon, as it is present after the zone cleaning, is melted in a quartz crucible nearly above the melting point of silicon. Now dopants (e.g. boron or phos-

phorus) can be added to the melt to achieve appropriate electrical characteristics of the single crystal.

A seed crystal (a perfect single crystal) on a rotating rod is brought to the surface of the silicon melt. This seed crystal pretends the orientation of the silicon crystal. In contact with the seed crystal, the melt overtakes its crystal structure. The fact that the crucible temperature is only slightly above the melting point of silicon, the melt solidifies immediately on the seed and the crystal grows.

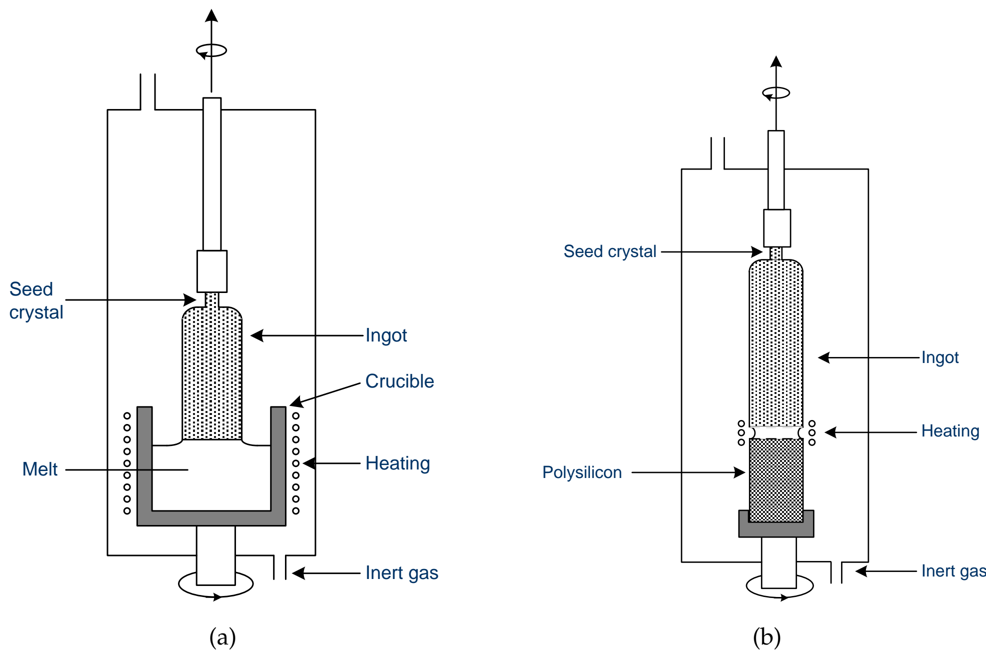


Fig. 1.3: Illustration of (a) the Czochralski and (b) the float-zone process

The seed is slowly pulled upward with constant rotation, while there is constant contact with the melt. The crucible turns in the opposite direction of the seed crystal. A constant temperature of the melt is essential to ensure a steady growth. The diameter of the single crystal is determined by the drawing speed, which provides 2 to 25 cm/h. The higher the drawing speed, the thinner the crystal. The entire apparatus is located in a controlled atmosphere, so that no oxidation of silicon can take place.

The disadvantage of this procedure is that the melt is accumulated with dopants during the process, since the dopants are more solubly in the melt than in the solid state. Thus the dopant concentration along the silicon rod is not constant. Also impurities or metals can dissolve from the crucible and built into the crystal.

The advantages of this method are the lower costs, and the ability to produce larger wafer sizes as in flot-zone processes.

1.3.3 Float-zone silicon

In contrast to the Czochralski process the polysilicon is not entirely molten, but, as in the zone cleaning, only a small area (a few millimeters).

Again, a seed crystal, which will be introduced to the end of the polycrystalline silicon rod, sets the crystal structure. The polycrystal is molten and assumes the structure of the seedling. The heated region is slowly guided along the rod, the polycrystalline silicon rod slowly transforms into a single crystal.

Since only a small portion of the polycrystalline silicon is molten, it can hardly be polluted (impurities accumulate at the bottom since their higher solubility). The doping is done by additions of dopants into the inert gas (eg with diborane or phosphine) which flows around the apparatus.

1.4 Wafer fabrication

1.4.1 Wafer separation and surface refinement

At first the single crystal is turned to a desired diameter and then bedight with one or two flats. The larger, first flat allows an precise alignment of the wafer during manufacturing. The second flat is used to detect the type of the wafer (crystal orientation, p-/n-type doped), but is not always used. Wafers with a diameter of 200 mm or above use a notch instead. This tiny notches on the edge of the disk also provide an alignment of the wafer, but take up much less costly wafer surface.

Sawing:
With an annular saw, whose cutting edge is filled with diamond splinters, the single crystal is sawn into thin discs = wafer. The saw provides a high accuracy during sawing without bumps. Up to 20 % of the crystal rod is lost due to the width of the saw blade. However, nowadays more often wire saws are used, in which multiple wafers can be cut at once from the staff. Therefore a long wire, which is wetted with a suspension of silicon carbide grains and a carrier (glycol or oil), is lead through rotating rollers. The

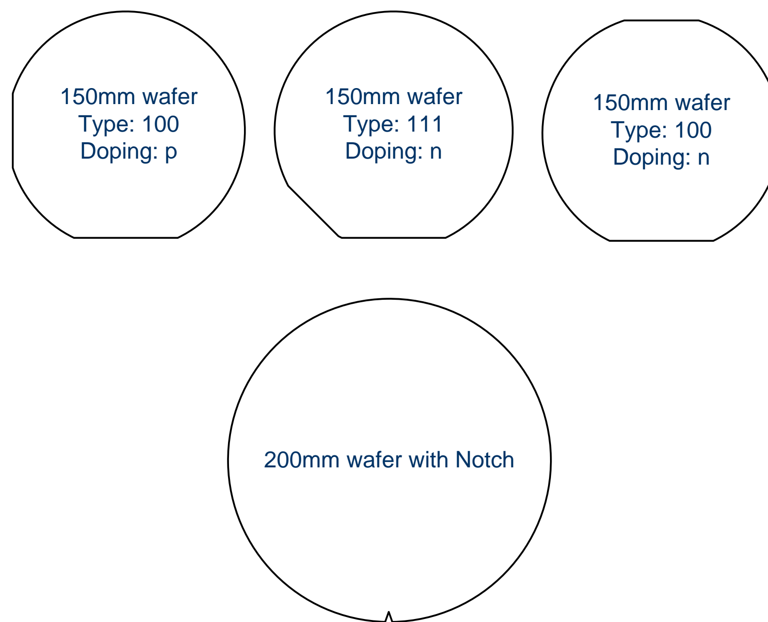


Fig. 1.4: Different types of wafers

silicon crystal is drained into the wire grid and thus cut into single wafers. The wire moves in counterstep with about 10 m/s and has a typically thickness of 0.1-0.2 mm.

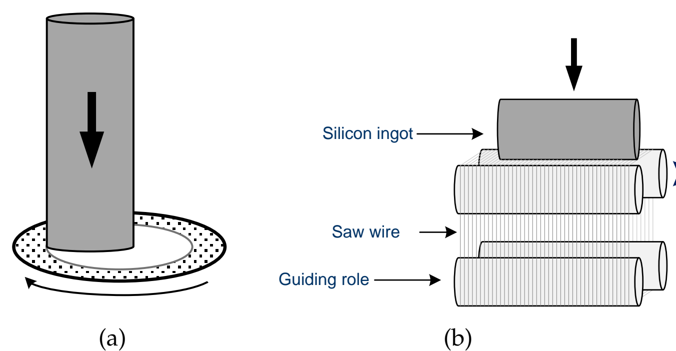


Fig. 1.5: Annular and wire saw

After sawing, the slices have a rough surface, and due to mechanical stress damages in the crystal lattice. For finishing the surface, the wafers pass several process steps.

Lapping:

Using granular abrasives (e.g. aluminum) 50 microns (0.05 mm) of the wafer surface are removed on a rotating steel disc. The grain size is reduced in stages, but the surface is re-injured due to the mechanical treatment. The flatness after lapping is about 2

microns.

Beveling of the edge:
In subsequent processes, the discs must have no sharp edges, as deposited layers may flake off otherwise. Therfore the bevel of the wafers are rounded with a diamond cutter.

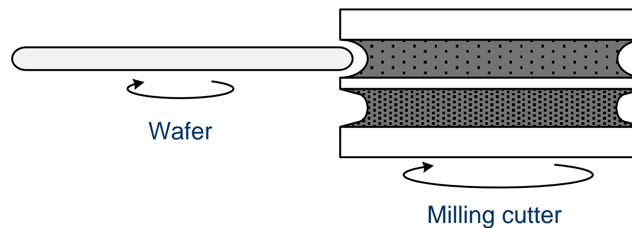


Fig. 1.6: Beveling

Etching:
In an additional wet etch process, with a mixture of hydrofluoric, acetic, and nitric acid, 50 microns are removed. Because this is a chemical process, the surface is not damaged. Crystal defects are permanently resolved.

Polishing:
This is the final step of surface refinement. At the end of the polishing step, the wafers do not have a bump of more than 3 nm (0.000003 mm). The wafers are treated with a mixture of sodium hydroxide NaOH, water, and silicon oxide grains. The oxide removes additional 5 microns from the surface, the hydroxide removes machining marks caused by the oxide grain.

1.4.2 Historical development of the wafer size

The manufacture of integrated circuits on silicon wafers started in the mid 1960s on wafers with a diameter of 25 mm. Nowadays, in modern semiconductor manufacturing wafers with a diameter of 150-300 mm are used. By 2012 the mass production of microchips on wafers with a diameter of 450 mm is expected; prototypes have already been produced for research purposes. The wafer surface is then increased by more than 300-fold of the tiny 1-inch wafer 50 years ago.

With larger wafers, the throughput rate increases significantly in the manufacture of microchips, whereby the cost is reduced accordingly in the production. Thus, with identical structure sizese more than twice as many chips can be produced on a 300 mm

Type	Diameter [mm]	Thickness [μm]	1st flat [mm]	Bowing [μm]
6 inch	150±0,5	≈700	55-60	25
8 inch	200±0,5	≈700	55-60	25
12 inch	300±0,5	≈700	55-60	25

Tab. 1.1: Typical data of wafers

wafer as on a 200 mm wafer. In addition, with increasing diameter the wafer's edge is less curved and thus the cut-off minimized (since chips are off rectangular shape).

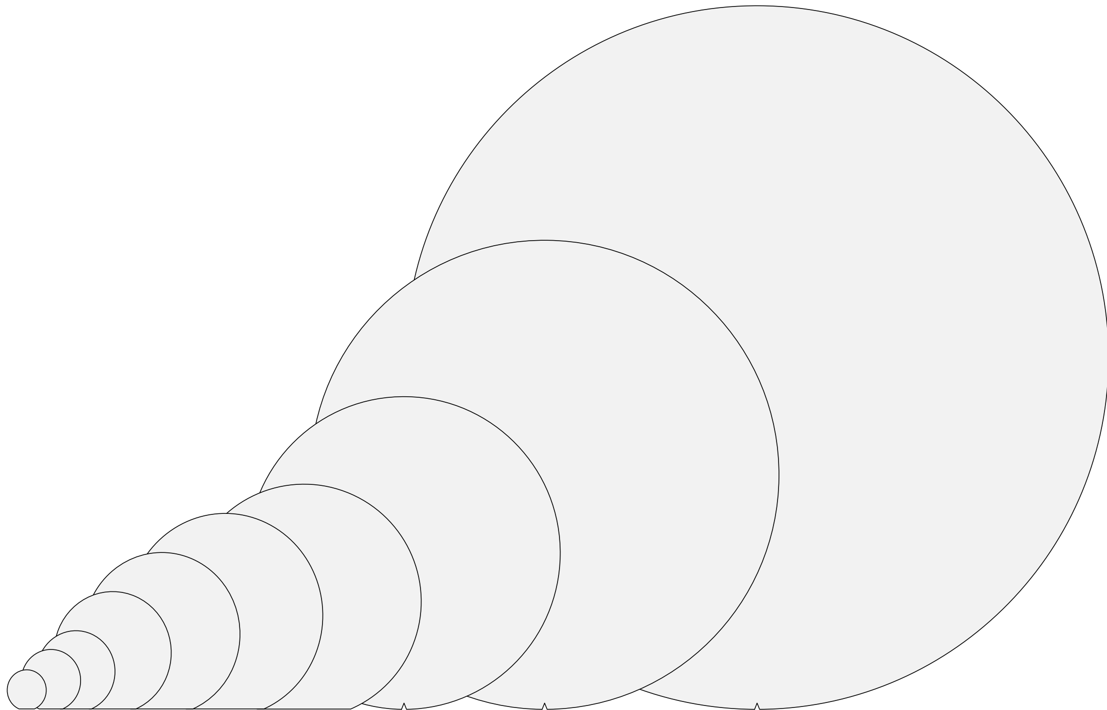


Fig. 1.7: Different wafer sizes: 25, 38, 51, 75, 100, 125, 150, 200, 300, 450 [mm] (drawn to scale)

1.5 Doping techniques

1.5.1 Definition

Doping means the introduction of impurities into the semiconductor crystal to deliberately change its conductivity due to deficiency or excess of electrons. In contrast to the doping during the wafer fabrication, where the entire wafer is doped, this article

describes the partial doping of silicon. The introduction of foreign substances can be achieved by diffusion, ion implantation (or alloy).

1.5.2 Diffusion

Molecular diffusion, often called simply diffusion, is a net transport of molecules from a region of higher concentration to one of lower concentration by random molecular motion. The result of diffusion is a gradual mixing of materials. To illustrate: a drop of ink in a glass of water is evenly distributed after a certain amount of time. In a silicon crystal, one finds a solid lattice of atoms through which the dopant has to move. This can be done in different ways:

- **Empty space diffusion:** the impurity atoms can fill empty places in the crystal lattice which are always present, even in perfect single crystals.
- **Inter lattice diffusion:** the impurity atoms move in-between the silicon atoms in the crystal lattice.
- **Changing of places:** the impurity atoms are located in the crystal lattice and are exchanged with the silicon atoms.

The dopant can diffuse as long as either a concentration gradient is balanced, or the temperature was lowered, so that the atoms can no longer move. The speed of the diffusion process depends on several factors:

- Dopant
- Concentration gradient
- Temperature
- Substrate
- crystallographic orientation of the substrate

Diffusion with an exhaustible source:
Diffusion with an exhaustible source means that the dopant is available in a limited amount only. The longer the diffusion process continues, the lower the concentration at the surface, and therefore the depth of penetration into the substrate increases. The diffusion coefficient of a substance indicates how fast it moves in the crystal. Arsenic

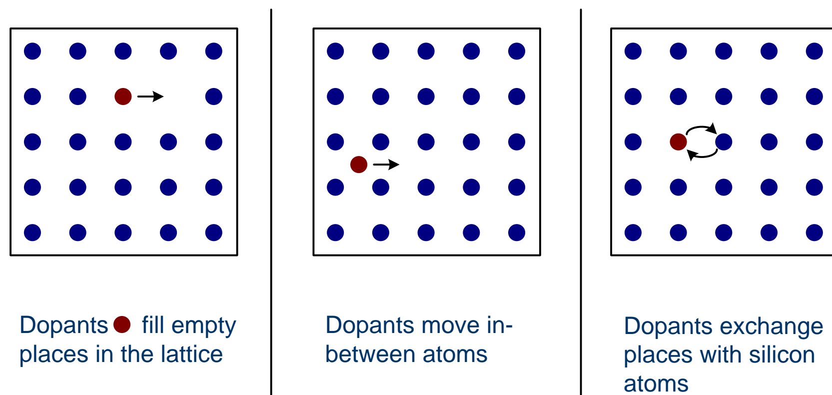


Fig. 1.8: Diffusion process

with a low diffusion coefficient penetrates slower into the substrate, as for example phosphorus or boron.

Diffusion with an inexhaustible source:
In diffusion processes with an inexhaustible source the dopants are available in unlimited amount, and therefore the concentration at the surface remains constant during the process. Particles that have penetrated into the substrate are continually replenished.

1.5.3 Diffusion methods

In the subsequent processes the wafers are placed in a quartz tube that is heated to a certain temperature.

Diffusion from the gas phase:
A carrier gas (nitrogen, argon, ...) is enriched with the desired dopant (also in gaseous form, e.g. phosphine PH_3 or diborane B_2H_6) and led to the silicon wafers, on which the concentration balance can take place.

Diffusion with solid source:
Slices which contain the dopants are placed in-between the wafers. If the temperature in the quartz tube is increased, the dopant from the source discs diffuses into the atmosphere. With a carrier gas, the dopant will be distributed uniformly, and thus reaches the surface of the wafers.

Diffusion with liquid source:
As liquid sources boron bromide BBr_3 or phosphoryl chloride $POCl_3$ can be used. A

carrier gas is led through the liquids and thus transporting the dopant in gaseous state. Since not the entire wafers should be doped, certain areas can be masked with silicon dioxide. The dopants can not penetrate through the oxide, and therefore no doping takes place at these locations. To avoid tensions or even fractions of the discs, the quartz tube is gradually heated (e.g. +10 °C per minute) till 900 C. Subsequent the dopant is led to the wafers. To set the diffusion process in motion, the temperature is then increased up to 1200 C.

Characteristic:

- since many wafers can be processed simultaneously, this method is quite favorable
- if there already are dopants in the silicon crystal, they can diffuse out in later processes due to high process temperatures
- dopants can deposit in the quartz tube, and be transported to the wafers in later processes
- dopants in the crystal are spreading not only in perpendicular orientation but also laterally, so that the doped area is enlarged in a unwanted manner

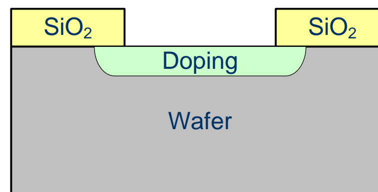


Fig. 1.9: Diffusion with an oxide mask

1.5.4 Ion implantation

In the ion implantation charged dopants (ions) are accelerated in an electric field and irradiated onto the wafer. The penetration depth can be set very precisely by reducing or increasing the voltage needed to accelerate the ions. Since the process takes place at room temperature, previously added dopants can not diffuse out. Regions that should not be doped, can be covered with a masking photoresist layer.

An implanter consists of the following components:

- **ion source:** the dopants in gaseous state (e.g. boron trifluoride BF_3) are ionized
- **accelerator:** the ions are drawn with approximately 30 kiloelectron volts out of the ion source
- **mass separation:** the charged particles are deflected by a magnetic field by 90 degrees. Too light/heavy particles are deflected more/less than the desired ions and trapped with screens behind the separator
- **acceleration lane:** several 100 keV accelerate the particles to their final velocity (200 keV accelerate bor ions up to 2.000.000 m/s)
- **Lenses:** lenses are distributed inside the entire system to focus the ion beam
- **distraction:** the ions are deflected with electrical fields to irradiate the desired location
- **wafer station:** the wafers are placed on large rotating wheels and held into the ion beam

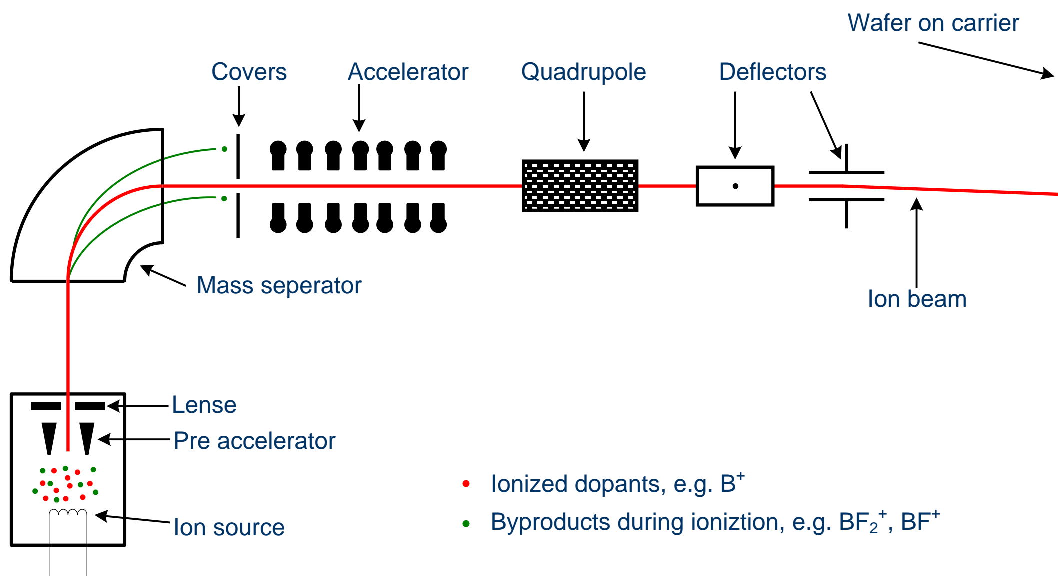


Fig. 1.10: Illustration of an ion implanter

Penetration depth of ions in the wafer:
In contrast to diffusion processes the particles do not penetrate into the crystal due to their own movement, but because of their high velocity. Inside the crystal they are

slowed down by collisions with silicon atoms. The impact causes damage to the lattice since silicon atoms are knocked from their sites, the dopants themselves are mostly placed interstitial. There, they are not electrically active, because there are no bonds with other atoms which may give rise to free charge carriers. The displaced silicon atoms must be re-installed into the crystal lattice, and the electrically inactive dopants must be activated.

Recovery the crystal lattice and activation of dopants:
Right after the implantation process, only about 5 % of the dopants are bond in the lattice. In a high temperature process at about 1000 °C, the dopants move on lattice sites. The lattice damage caused by the collisions have already been cured at about 500 °C. Since the dopants move inside the crystal during high temperature processes, these steps are carried out only for a very short time.

Channeling:
The substrate is present as a single crystal, and thus the silicon atoms are regularly arranged and form "channels". The dopant atoms injected via ion implantation can move parallel to these channels and are slowed only slightly, and therefore penetrate very deeply into the substrate. To prevent this, there are several possibilities:

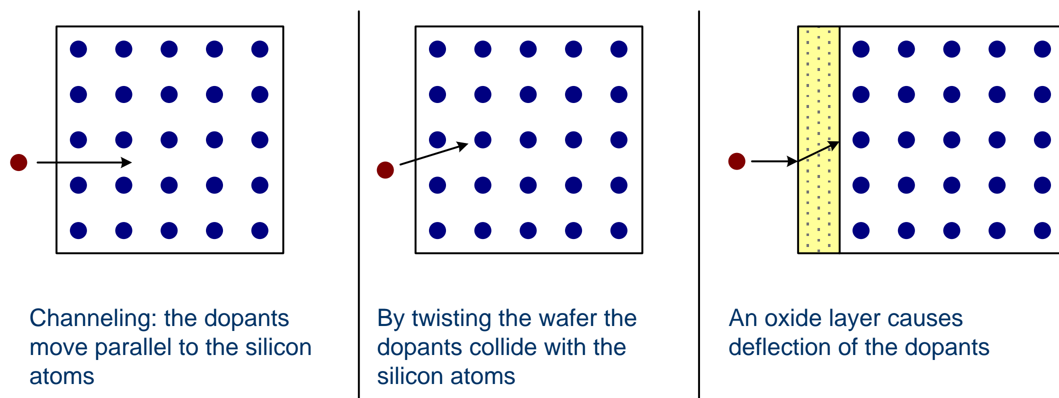


Fig. 1.11: Channeling effect in the ingot

- **Wafer alignment:** the wafers are deflected by about 7° with respect to the ion beam. Thus the radiation is not in parallel direction to the channels and the ions are decelerated by collisions immediately.
- **Scattering:** on top of the wafer surface a thin oxide is applied, which deflects the ions, and therefore prevents a parallel arival

Characteristic:

- the reproducibility of ion implantation is very high
- the process at room temperature prevents the outward diffusion of other dopants
- spin coated photoresist as a mask is sufficient, an oxide layer, as it is used in diffusion processes, is not necessary
- ion implanters are very expensive, the costs per wafer are relatively high
- the dopants do not spread laterally under the mask (only minimally due to collisions)
- nearly every element can be implanted in highest purity
- previous used dopants can deposit on walls or screens inside the implanter and later be carried to the wafer
- three-dimensional structures (e.g. trenches) can not be doped by ion implantation
- the implantation process takes place under high vacuum, which must be produced with several vacuum pumps

There are several types of implanters for small to medium doses of ions (10^{11} to 10^{15} $ions/cm^2$) or for even higher doses of 10^{15} to 10^{17} $ions/cm^2$.

The ion implantation has replaced the diffusion mostly due to its advantages.

Doping using alloy
For completeness it should be mentioned that besides ion implanation and diffusion there is an alternative process: doping using alloy. Since this procedure has disadvantages such as cracks in the substrate, it is not used in today's semiconductor technology any more.